Claims:

1. A device for area efficient realization of coefficient, said device comprising architecture [A] with hardware sharing techniques and optimization applied to this architecture, the architecture [A] is connected to coefficient lines CLin_0, CLin_1.....CLin_n and/or BLin_0, BLin_1,....BLin_n coming from block [E] and/or [F], to be connected to perform filtering operation or a mathematical computing operation with optimization in hardware and provides a zero latency clock output, the serial input bit line of said architecture [A] are S1, S2,.....Sn. [where n represents the number of coefficients of the filter], the addition terms of the equation [(a0*S1+b0*S2+....+k0*Sn), (a1*S1+b1*S2+.....+k1*Sn).....(am*S1+bm*S2+.....+km*Sn)] are represented as blocks [B], the said block [B] is a combinational block consisting of full adders (FA) & full subtractor (FS) elements, the values a0, b0,..... etc. are (+ / -1 or 0), the connection of elements (FA/FS) to S1, S2....Sn lines and interconnection of the elements (FA,FS) depend on the value of coefficients, the final output of last element [FA/FS] of each block [B] is terminated through lines b_1, b_2,....b_m at [T] elements, the number of T elements in cluster [C] depends on the size of maximum coefficient value and is share-able for all the coefficient in the coefficient architecture [A], in the said architecture all the combinational elements [B] are clustered together as [D] and all the unit delay elements {T[1], T[2].....T[m]} are clustered together in [C], thereby separating the sequential and combinational logic, In the said architecture [A] the output of element [T] is connected to the one of the inputs of combinational logic of block [B] of next bit position, the interconnections from cluster [C] to [B] is represented as t_1, t_2,.....t_m, the elements [FA/FS] are arranged in matrix form FA0_0 to FA0_n in bit position 0, FA1_1 to FA1_n in bit position 1,.... FAm_1 to FAm_n in bit position m whose presence is defined by coefficient value, the carry-out pin of full

adder (FA) of each cluster stage[B] in the said architecture [A] is fed to input of full adder (FA) of previous stage cluster [B] i.e stage preceding the flip-flop (T) element of cluster [C], in this way the same Flip-Flop [T] (T1, T2, T3... Tn) is used for multiplication by "a factor of two" and also in the implementation of the carry structure in the one bit serial adder, in the said architecture some extra components represented as block [Ex] are being used for connecting the carryout of all the adders/subtractors [FA/FS] of last stage of [D], the element [FA/FS] and [T] are used within this block, and hence, the said architecture [A] structures the circuit into sequential block [C] consisting of [T] elements and combinational [D] consisting of [FA,FS] elements, while the [T] elements of block [C], are common for all the coefficients and are share-able and positioned at end position of each block [B], the Block [D] has combinational element block[B] which are essentially [FA,FS], thereby making share-able hardware within block [D] and the final output is the output of BITm position.

2. The device as claimed in claim1 wherein provides the area minimal realization of digital filters based on coefficient architecture [A], when operated in bit serial fashion, the device provides hardware minimization for finite impulse response(FIR) filter, infinite impulse response filter(IIR) and for other filters and applications related to combinational logic consisting of delay element(T), multiplier(M), adder and subtractor.

3. The device as claimed in claim1 wherein further optimization technique in cluster [D] is done by using common adders (FA) and common subtractor (FS) and using this shared outputs.

4. The device as claimed in claim1 wherein further optimization technique in cluster [D] is done by using subtractor (FS) instead of adders, when the coefficient value is closer to power of two.

Sub A1

5. The device as claimed in claim1 wherein further optimization technique in cluster [D] is done by minimizing the use of subtractor by taking common subtraction operator and using adder instead.

6. The device as claimed in one of the previous claims (1-5) wherein when used in implementation 2 of FIR/IIR filter and similar structure of filters, results in quite area efficient realization of the filter, the storage area in implementation2, referred as delay elements [Z^{-1}], is smaller as compared to implementation 1 which is present due to inherent property of the structure of implementation 2, and an additional saving in area in filter coefficient realization design is achieved by using the claimed structure of coefficient architecture [A] of "Figure 12".

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